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10/813,040	03/29/2004	Ralph James	501292.01 (30263/US)	4142
27076 7590 02/14/2008 DORSEY & WHITNEY LLP INTELLECTUAL PROPERTY DEPARTMENT SUITE 3400 1420 FIFTH AVENUE SEATTLE, WA 98101			EXAMINER YUEN, KAN	
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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

## Office Action Summary

Application No.

10/813,040

Applicant(s)

JAMES, RALPH

Examiner

Kan Yuen

Art Unit

2616

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 26 November 2007.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-44 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-14, 22, 30 and 39 is/are rejected.
- 7) ☒ Claim(s) 15-21, 23-29, 31-38, 40-44 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/ are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- ☒ Notice of References Cited (PTO-892)
- ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- ☒ Information Disclosure Statement(s) (PTO/SB/08)  
Paper No(s)/Mail Date 11/26/2007.
- ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_
- ☐ Notice of Informal Patent Application
- ☐ Other: \_\_\_\_\_

### ***Response to Arguments***

1. Applicant's arguments filed on 11/26/2007 have been fully considered but they are not persuasive. Applicant argued in claims 1 and 6 that Holmberg patent did not teach a method of synchronizing memory hubs for processing functional memory commands. However, as shown in fig. 2A-2D. When the synchronizing message reaches the last slave node, the last slave node will transmit the message back to the master node to notify the master node that all slave nodes are now synchronized. The master node may then transmit the download network message 50, which includes number of nodes field 54, and therefore the message 50 is considered as a memory command.

### ***Double Patenting***

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a

terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 1 and 6 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 79 of copending Application No. 11433131. Although the conflicting claims are not identical, they are not patentably distinct from each other because of the following.

For claims 1 and 6, claim 79 of copending application no. 11433131 disclosed the method of synchronizing communication links in a memory hub having upstream and downstream reception ports and upstream and downstream transmission ports, each port coupled to a corresponding port to form a transmission-reception port pair, the method comprising: synchronizing a receive clock signal relative to reception of data for the transmission-reception port pair including the downstream reception port; synchronizing a receive clock signal relative to reception of data for the transmission-reception port pair including the upstream reception port subsequent to synchronizing the transmission-reception port pair including the downstream reception port; synchronizing a receive clock signal relative to reception of data for the transmission-reception port pair including the downstream transmission port subsequent to synchronizing the transmission-reception port pair including the downstream reception port and prior to synchronizing the transmission-reception port pair including the upstream reception port; and synchronizing a receive clock signal relative to reception of data for the transmission-reception port pair including the upstream transmission port subsequent to synchronizing the transmission-reception port pair including the upstream

reception port.

However, when the prior art device or method is the same as a device or method described in the applicant's present specification for carrying out the claimed method, it can be assumed the device will inherently perform the claimed process (see MPEP section 2112.02 Process claims). Thus, it would have been obvious to a person in an ordinary skill in the art at the time of the invention to use the obviousness in the network of the co-pending application. The motivation for using the method being that it provides system reliability.

Claim 14 is provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 45 of copending Application No. 11433131. Although the conflicting claims are not identical, they are not patentably distinct from each other because of the following.

For claim 14, claim 45 of copending application no. 11433131 disclosed the method of downstream and upstream reception ports, each reception port operable in an initialization mode to synchronize reception of test data from a respective off-hub transmission port and further operable to enter a normal mode in response to receiving an enable command from the respective off-hub transmission port, each reception port operable to generate a completion signal in response to receiving inverted test data from the respective off-hub transmission port and further operable to generate an enable signal in response to receiving an enable command from the respective off-hub transmission port; and downstream and upstream transmission ports, each transmission port operable in the initialization mode to synchronize transmission of test data to a

respective off-hub reception port and further operable to enter the normal mode in response to receiving an enable signal from a respective on-hub reception port, each transmission port operable to transmit inverted test data to the respective off-hub reception port in response to receiving a completion signal from the respective on-hub reception port and operable to generate an enable command for the respective off-hub reception port in response to receiving an enable signal from the respective on-hub reception port.

However, when the prior art device or method is the same as a device or method described in the applicant's present specification for carrying out the claimed method, it can be assumed the device will inherently perform the claimed process (see MPEP section 2112.02 Process claims). Thus, it would have been obvious to a person in an ordinary skill in the art at the time of the invention to use the obviousness in the network of the co-pending application. The motivation for using the method being that it provides system reliability.

Claim 22 is provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 64 of copending Application No. 11433131. Although the conflicting claims are not identical, they are not patentably distinct from each other because of the following.

For claim 22, claim 64 of copending application no. 11433131 disclosed the method of a plurality of memory devices; and a memory hub comprising: downstream and upstream reception ports, each reception port operable in an initialization mode to synchronize reception of test data from a respective off-hub transmission port and

further operable to enter a normal mode in response to receiving an enable command from the respective off-hub transmission port, each reception port operable to generate a completion signal in response to receiving inverted test data from the respective off-hub transmission port and further operable to generate an enable signal in response to receiving an enable command from the respective off-hub transmission port; and downstream and upstream transmission ports, each transmission port operable in the initialization mode to synchronize transmission of test data to a respective off-hub reception port and further operable to enter the normal mode in response to receiving an enable signal from a respective on-hub reception port, each transmission port operable to transmit inverted test data to the respective off-hub reception port in response to receiving a completion signal from the respective on-hub reception port and operable to generate an enable command for the respective off-hub reception port in response to receiving an enable signal from the respective on-hub reception port. Although the co-pending application did not claim the local hub circuitry coupled to the interfaces and to the memory device.

However, when the prior art device or method is the same as a device or method described in the applicant's present specification for carrying out the claimed method, it can be assumed the device will inherently perform the claimed process (see MPEP section 2112.02 Process claims). Thus, it would have been obvious to a person in an ordinary skill in the art at the time of the invention to use the obviousness in the network of the co-pending application. The motivation for using the method being that it provides system reliability.

Claim 30 is provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 69 of copending Application No. 11433131. Although the conflicting claims are not identical, they are not patentably distinct from each other because of the following.

For claim 30, claim 69 of copending application no. 11433131 disclosed the method of a system controller; a plurality of memory modules, each memory module being coupled to adjacent memory modules through respective high-speed communications links, at least one of the memory modules being coupled to the system controller through a respective high-speed; communications link, and each memory module comprising: a plurality of memory devices; and a memory hub, comprising: downstream and upstream reception ports, each reception port operable in an initialization mode to synchronize reception of test data from a respective off-hub transmission port and further operable to enter a normal mode in response to receiving an enable command from the respective off-hub transmission port; each reception port operable to generate a completion signal in response to receiving inverted test data from the respective off-hub transmission port and further operable to generate an enable signal in response to receiving an enable command from the respective off-hub transmission port; and downstream and upstream transmission ports, each transmission port operable in the initialization mode to synchronize transmission of test data to a respective off-hub reception port and further operable to enter the normal mode in response to receiving an enable signal from a respective on-hub reception port, each transmission port operable to transmit inverted test data to the respective off-hub



reception port in response to receiving a completion signal from the respective on-hub reception port and operable to generate an enable command for the respective off-hub reception port in response to receiving an enable signal from the respective on-hub reception port.

However, when the prior art device or method is the same as a device or method described in the applicant's present specification for carrying out the claimed method, it can be assumed the device will inherently perform the claimed process (see MPEP section 2112.02 Process claims). Thus, it would have been obvious to a person in an ordinary skill in the art at the time of the invention to use the obviousness in the network of the co-pending application. The motivation for using the method being that it provides system reliability.

Claim 39 is provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 74 of copending Application No. 11433131. Although the conflicting claims are not identical, they are not patentably distinct from each other because of the following.

For claim 39, claim 74 of copending application no. 11433131 disclosed the method of a processor; a system controller coupled to the processor through respective downstream and upstream high-speed communications links; a memory system, comprising: a system controller; a plurality of memory modules, each memory module being coupled to adjacent memory modules through respective high-speed communications links, at least one of the memory modules being coupled to the system controller through a respective high-speed communications link, and each memory

module comprising: a plurality of memory devices; downstream and upstream reception ports, each reception port operable in an initialization mode to synchronize reception of test data from a respective off-hub transmission port and further operable to enter a normal mode in response to receiving an enable command from the respective off-hub transmission port, each reception port operable to generate a completion signal in response to receiving inverted test data from the respective off-hub transmission port and further operable to generate an enable signal in response to receiving an enable command from the respective off-hub transmission port; and downstream and upstream transmission ports, each transmission port operable in the initialization mode to synchronize transmission of test data to a respective off-hub reception port and further operable to enter the normal mode in response to receiving an enable signal from a respective on-hub reception port, each transmission port operable to transmit inverted test data to the respective off-hub reception port in response to receiving a completion signal from the respective on-hub reception port and operable to generate an enable command for the respective off-hub reception port in response to receiving an enable signal from the respective on-hub reception port.

However, when the prior art device or method is the same as a device or method described in the applicant's present specification for carrying out the claimed method, it can be assumed the device will inherently perform the claimed process (see MPEP section 2112.02 Process claims). Thus, it would have been obvious to a person in an ordinary skill in the art at the time of the invention to use the obviousness in the network of the co-pending application. The motivation for using the method being that it provides

system reliability.

***Claim Rejections - 35 USC § 102***

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 2 are rejected under 35 U.S.C. 102(b) as being anticipated by Holmberg et al. (Pat No.: 4982485).

For claim 1, Holmberg et al. disclosed the method of synchronizing an upstream and downstream link coupled to the controller (see column 2, lines 32-45, and see fig. 1); sequentially synchronizing downstream links starting with the downstream link coupled between the controller and the first hub (see column 7, lines 1-30, and see fig. 1, and fig. 2A-D). The master node 11, and a plurality of 12A-12N slave nodes are shown in fig. 1. The master node starts to sequentially synchronizing the link 13A through link 13 (N+1). We can interpret that the links from 13A through 13 (i) are the downstream links, and from link 13 (i+1) through link 13 (N+1) are the upstream links. The master node can be considered as the controller, and the slave nodes can be considered as the memory hubs; sequentially synchronizing upstream links starting with the upstream link coupled between the last memory hub and the next upstream hub (see column 7, lines 1-30, and see column 8, lines 5-25, and see fig. 1, and fig. 2A-D).

The upstream synchronization is started in the link 13 ( $i+1$ ) between the slave node 12 ( $i$ ) and slave node 12 ( $i+1$ ); providing an indication to the controller when the upstream link between the first and second hubs has been synchronized (see column 5, lines 57-67, column 6, lines 1-2, and see column 8, lines 5-25, and see fig. 1, and fig. 2A-D).

Fig2 A-D shown four types of messages originated by the master node. The data transfer message shown in fig. 2D is transmitted based on the synchronization message. The data transfer message is transmit to slave node 12A, and node 12A will pass it on to the next slave node until it reaches back to the master node, which indicates that all slaves nodes have received it; sequentially enabling downstream links to process functional memory commands; sequentially enabling upstream links to process functional memory commands, and providing an indication to the controller that all links have been enabled (see column 6, lines 35-58, see column 8, lines 49-65, and see fig. 1, and fig. 2A-D). The download network message enables the slave nodes 12 to determine their respective positions in the system; where determining their respective positions can help each node the self-configuring to adjust delay time to perform measurements in synchronism.

Regarding claim 2, Holmberg et al. also disclosed the method of synchronizing each of the links comprises applying test data signals over the links, and adjusting a phase shift of a generated receive clock signal relative to the data signals (see column 8, lines 49-65, and see fig. 1, and fig. 2A-D). The network parameter message 50 is considered as a test signal which being transmitted to the slave nodes. The signal

enables the slave nodes to determine their respective position of time delay, so that it can adjust the delay time for synchronism respectively.

***Claim Rejections - 35 USC § 103***

4. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 6, 7 are rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Holmberg et al. (Pat No.: 4982485).

Regarding claim 6, Holmberg et al. also disclosed the method of synchronizing each upstream and downstream link; in a counter-clockwise order starting with the downstream link coupled between the controller and the first memory module, signaling

to the next adjacent clockwise link that the prior clockwise link has been synchronized (see column 7, lines 1-30, and see fig. 1, and fig. 2A-D). The master node 11, and a plurality of 12A-12N slave nodes are shown in fig. 1. The master node starts to sequentially synchronizing the link 13A through link 13 (N+1). We can interpret that the links from 13A through 13 (i) are the downstream links, and from link 13 (i+1) through link 13 (N+1) are the upstream links. The master node can be considered as the controller, and the slave nodes can be considered as the memory hubs. When each slave node receives the synch message 60, it establish a delay time period, and then forwards the message to the next slave node. Therefore it can be interpreted as signaling to the next node that the previous link has been synchronized; detecting through the upstream link coupled between the controller and the first memory module when all links have been synchronized (see column 5, lines 57-67, column 6, lines 1-2, and see column 8, lines 5-25, and see fig. 1, and fig. 2A-D). Fig2 A-D shown four types of messages originated by the master node. The data transfer message 70 shown in fig. 2D is transmitted based on the synchronization message. The data transfer message is transmit to slave node 12A, and node 12A will pass it on to the next slave node until it reaches back to the master node. The master node detects to receive the message 70 return back, so that it knows all slaves nodes have received it; in a counter-clockwise order starting with the downstream link coupled between the controller and the first memory module, enabling each link; and detecting through the upstream link coupled between the controller and the first memory module when all links have been enabled (see column 6, lines 35-58, see column 8, lines 49-65, and see fig. 1, and fig. 2A-D).

The download network message 50 enables the slave nodes 12 to determine their respective positions in the system; where determining their respective positions can help each node the self-configuring to adjust delay time to perform measurements in synchronism. The master node waits for the network message 50 to return so that it knows all slave nodes have received this message. Although Holmberg et al. did not disclose the method of clockwise order, however it is skill in the art to either perform in counter-clock or clock order. Thus, it would have been obvious to the person of ordinary skill in the art at the time of the invention to use the obviousness in the network of Holmberg et al. The motivation for using the obviousness in the network of Holmberg being that it increases the flexibility of the network; Transferring and receiving functional memory commands from the control after all links have been enable (column 6, lines 35-67).

Regarding claim 7, Holmberg et al. also disclosed the method of synchronizing each of the links comprises applying test data signals and adjusting a phase shift of a generated receive clock signal relative to the data signals (see column 8, lines 49-65, and see fig. 1, and fig. 2A-D). The network parameter message 50 is considered as a test signal which being transmitted to the slave nodes. The signal enables the slave nodes to determine their respective position of time delay, so that it can adjust the delay time for synchronism respectively.

7. Claims 3-5, 8-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Holmberg et al. (Pat No.: 4982485), in view of Miyazaki (Pat No.: 4078228).

For claim 3, Holmberg disclosed all the subject matter of the claimed invention with the exception of inverting the test data signals and providing the inverted test data signals over the upstream link coupled to the controller. Miyazaki from the same or similar fields of endeavor teaches the method of inverting the test data signals and providing the inverted test data signals over the upstream link coupled to the controller (see column 12, lines 57-68, and column 13, lines 1-10, and see fig. 11). In fig. 11, the inverter 412 inverted incoming signal to gate 413. Thus, it would have been obvious to the person of ordinary skill in the art at the time of the invention to use the method as taught by Miyazaki in the network of Holmberg et al. The motivation for using the method as taught by Miyazaki in the network of Holmberg et al., being that the method enhances the balance of data distribution in the system.

Regarding claim 4, Miyazaki disclosed the method of providing an indication to the controller that all links have been enabled comprises providing an enablement command over the upstream link coupled to the controller (see column 12, lines 57-68, and column 13, lines 1-10, and see fig. 11). The battery 416 is provided to generate an enablement signal to supplies the station shown in fig. 11 in operation or normal mode;

Regarding claim 5, Miyazaki disclosed the method of the enablement command comprises a NOP command (see column 12, lines 57-68, and column 13, lines 1-10, and see fig. 11). The battery 416 is provided to generate an enablement signal to supplies the station shown in fig. 11 in operation or normal mode;



Regarding claim 8, Miyazaki disclosed the method of signaling to the next adjacent clockwise link that the prior clockwise link has been synchronized comprises providing an inversion signal to next adjacent clockwise link (see column 12, lines 57-68, and column 13, lines 1-10, and see fig. 11). In fig. 11, the inverter 412 inverted incoming signal to gate 413.

Regarding claim 9, Miyazaki disclosed the method of in response to the inversion signal inverted test data signals are applied over the next adjacent link (see column 12, lines 57-68, and column 13, lines 1-10, and see fig. 11). In fig. 11, the inverter 412 inverted incoming signal to gate 413.

Regarding claim 10, Miyazaki disclosed the method of each link includes a transmission port and a reception port, and wherein enabling each link comprises first enabling the transmission port and thereafter enabling the reception port (see column 12, lines 57-68, and column 13, lines 1-10, and see fig. 11). The battery 416 is provided to generate an enablement signal to supplies the station shown in fig. 11 in operation or normal mode;

Regarding claim 11, Miyazaki disclosed the method of the reception port in each link is enabled by the transmission port applying an enable command to the reception port (see column 12, lines 57-68, and column 13, lines 1-10, and see fig. 11).

Regarding claim 12, Miyazaki disclosed the method of the enable command comprises a NOP command (see column 12, lines 57-68, and column 13, lines 1-10, and see fig. 11). The battery 416 is provided to generate an enablement signal to supplies the station shown in fig. 11 in operation or normal mode;

Regarding claim 13, Miyazaki disclosed the method of once the reception port of a given link has been enabled, an enable signal is supplied to the transmission port of the next adjacent clockwise port to thereby enable the transmission port of the next adjacent clockwise port (see column 12, lines 57-68, and column 13, lines 1-10, and see fig. 11). The battery 416 is provided to generate an enablement signal to supplies the station shown in fig. 11 in operation or normal mode.

#### ***Allowable Subject Matter***

8. Claims 15-21, 23-29, 31-38, 40-44 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

#### ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kan Yuen whose telephone number is 571-270-1413. The examiner can normally be reached on Monday-Friday 10:00a.m-3:00p.m EST.

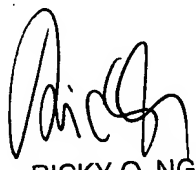
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ricky O. Ngo can be reached on 571-272-3139. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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KY

  
RICKY Q. NGO  
SUPERVISORY PATENT EXAMINER